Patent claims

1. A method for producing a semiconductor wafer with a number of semiconductor chips (2) for a number of electronic components (1), the method comprising the following method steps:

- providing a semiconductor wafer (13), arranged in rows and columns, with a number of semiconductor chip positions,
- creating an active surface area (5) in the semiconductor chip positions on the active top side (4) of the semiconductor wafer (13) and applying contact connecting areas (6) outside the active surface area (5),
- applying and patterning a sacrificial layer (21) which comprises insulation material, on the active surface area (5), leaving through openings (22) in the sacrificial layer (21) exposed in the edge areas of the active surface area (5),
- applying a conductive material to the sacrificial layer (21) and into the through openings (22) for forming a cover layer (9) with through lines (10),
- removing the sacrificial layer (21) by forming a self-supporting cover layer (9), supported by through lines (22), above a hollow space (11) above the active surface area (5),
- applying and patterning a first plastic layer (15) on the cover layer (9) and on the active top side (4), leaving the contact connecting areas (6) exposed and sealing side edges (23) of the hollow space (11) above the active surface area (5),
- applying external contacts (14) to the contact connecting areas (6),
- splitting the semiconductor wafer (13) into individual electronic components (1).

2. The method as claimed in claim 1, wherein the sacrificial layer (21) is deposited on the semiconductor wafer (13) from a chemical gas phase,

forming silicon oxide or silicon nitride, or as a photoresist layer on the semiconductor wafer (13).

3. The method as claimed in claim 1 or 2, wherein, after a cover layer (9) comprising a polycrystalline silicon has been applied, a sacrificial layer (21) comprising silicon oxide is removed by means of hydrofluoric acid.

4. The method as claimed in one of claims 1 to 3, wherein, after a metallic cover layer (9) of preferably nickel, copper, aluminum or alloys thereof has been applied, a sacrificial layer (21) comprising photoresist is removed by means of a solvent.

5. The method as claimed in one of claims 1 to 4, wherein, onto the first plastic layer (15) a rewiring pattern (16) is applied which connects the contact connecting areas (6) to external contact areas (18) and then a second plastic layer (20) is applied, leaving the external contact areas (18) exposed.

6. An electronic component having the following features:

- a semiconductor chip (2), comprising
  - a semiconductor substrate (3),
  - an active top side (4) on the semiconductor substrate (3),
  - an active surface area (5) on the active top side (4) and
  - contact connecting areas (6) which are electrically connected to the active surface area (5),
  - a package (7) which comprises a package-forming plastic layer (8) which covers the substrate (3) leaving the contact connecting areas (6) exposed,
  - a self-supporting electrically conductive cover layer (9) which is arranged above the active

surface area (5) and which is supported on through lines (10) to the active top side (4) and forms a hollow space (11) between the active surface area (5) and cover layer (9), the height of the hollow space (11) corresponding to the thickness of an insulation layer (12), photoresist layer or metal layer normal for semiconductor wafers (13).

7. The electronic component as claimed in claim 6, wherein the cover layer (9) has a thickness (d) which corresponds to a thickness of conductor tracks on a semiconductor wafer (13).

8. The electronic component as claimed in claim 6 or claim 7, wherein the contact connecting areas (6) are arranged outside the active surface area (5) and comprise external contacts (14) of the electronic component (1).

9. The electronic component as claimed in one of claims 6 to 8, wherein the package-forming plastic layer (8) covers the cover layer (9), leaving the contact connecting areas (6) exposed, and seals the hollow space (11) on the side between the through lines (10).

10. The electronic component as claimed in one of claims 6 to 9, wherein, on a first plastic layer (15), a rewiring pattern (16) with rewiring lines (17) is arranged which lead from the contact connecting areas (6) to external contact areas (18), external contacts (19) being arranged on the external contact areas (18), and a second plastic layer (20) is arranged on the first plastic layer (15), leaving the external contacts (19) exposed and embedding the rewiring pattern (17).

11. The electronic component as claimed in one of claims 6 to 10, wherein the through lines (19) are

arranged regularly distributed around the circumference of the cover layer (9).

12. The electronic component as claimed in one of claims 6 to 11, wherein the cover layer (9) comprises a metal or a semiconductor material, preferably heavily doped polycrystalline silicon.

13. The electronic component as claimed in one of claims 6 to 12, wherein the active surface area (5) comprises a sensor in MEM structure, a filter, a microphone or microfabricated effectors.

14. The electronic component as claimed in one of claims 6 to 13, wherein the active surface area (5) comprises a front-end module of a mobile telephone or a power amplifier module of the mobile telephone and/or an amplifier module for structure-borne acoustic waves or an amplifier module for surface acoustic waves.

15. A semiconductor wafer which comprises electronic components (1) arranged in rows and columns, according to one of claims 1 to 9.

16. An application which comprises electronic components (1), arranged in rows and columns, according to one of claims 1 to 9.